An Indium Phosphide MMIC Amplifier for 180–205 GHz

John W. Archer, *Fellow, IEEE*, Richard Lai, *Member, IEEE*, Ron Grundbacher, Mike Barsky, Roger Tsai, and Phil Reid

***Abstract*—This paper describes a high-performance Indium Phosphide (InP) monolithic microwave integrated circuit (MMIC) amplifier, which has been developed for application in radio-astronomy and imaging-array receivers. Implemented using co-planar waveguide, the six-stage amplifier exhibits 15 dB gain, 10 dB input and output return loss, and low noise figure over the 180–205 GHz frequency range. Only one design pass was needed to obtain excellent agreement between the predicted and measured characteristics of the circuit, a unique achievement in this frequency band. The circuit is also the first 180–205 GHz amplifier designed for and successfully fabricated using TRW's standard 0.1–μm InP HEMT process.**

***Index Terms*—Coplanar waveguides, InP, low-noise amplifiers, millimeter-wave amplifiers, MMICs.**

I. Introduction

INDIUM PHOSPHIDE (InP)-based high electron mobility transistors (HEMT's) have demonstrated the highest gain, lowest noise figure, and highest frequency capability of any three-terminal transistor [1]–[3] and are attractive for next generation satellite communication systems, wireless LAN, and high-requency remote sensing applications. This paper describes the design and performance of a 180–205 GHz low-noise amplifier monolithic microwave integrated circuit (MMIC). Only a single design pass was required to achieve performance comparable with the only other amplifier reported in this band [4]. This MMIC was developed for a demonstration millimeter-wave imaging-array receiver with potential application in passive, radiometric imaging for commercial remote-sensing and in radio-astronomy. The millimeter-wave MMIC's, designed and tested at CSIRO, were fabricated under contract by TRW Inc. using a state-of-the-art 0.1-μm InP HEMT process [5]. CSIRO's unique opportunity for early access to this leading-edge InP technology is helping TRW expedite InP's maturity and commercial availability.

II. The Fabrication Process

TRW's InP HEMT MMIC process evolved from an existing, space-qualified GaAs HEMT MMIC process, taking advantage of an established knowledge base in this more mature technology [6]. For the MMIC's discussed in this paper, the wafers were grown by molecular-beam epitaxy on 75 mm diameter Fe-doped semi-insulating substrates. The epitaxial structure uses a 200-Å pseudomorphic InGaAs channel with 60% indium. The main features of the process are 0.1-μm gates defined by electron-beam lithography, 750-Å plasma-enhanced chemical vapor deposited silicon nitride for device passivation, 100 $\Omega/\square$ nichrome thin-film resistors, and 300 pF/mm^2 silicon nitride metal–insulator–metal capacitors. The wafers are thinned to 75 μm and 40 μm diameter, through-substrate via holes are etched using a dry process. Ti/Au backside metallization is sputtered/plated to a thickness of 3.5 μm. For the four production wafers fabricated for CSIRO, typical 0.1-μm InP HEMT devices exhibited f_t in the range 184–196 GHz at 1 V drain bias (test device geometry was two-finger, 200 μm total gate width). The peak transconductance for the test devices across these four wafers varied from 986 to 1049 mS/mm. This data highlights the high-gain, high-frequency performance and excellent wafer-to-wafer device uniformity achieved by TRW's process.

III. The Amplifiers

The 180–205 GHz HEMT amplifier reported here was a six-stage design, as shown in Fig. 1, implemented in coplanar waveguide on the semi-insulating InP substrate. The circuit was designed using COPLAN, a simulation tool developed by IMST GmbH for the design of coplanar waveguide MMIC's within the HP-Eesof Series IV software. COPLAN utilizes an efficient finite-difference method for the accurate electro-magnetic modeling of three-dimensional coplanar circuit elements. The effects of metallization thickness, air-bridges and process-related parameters are taken into account during the simulation. In order to achieve first-pass design success, CSIRO has found that it is essential to carefully evaluate the validity of the coplanar element models with respect to the allowable range of transmission line widths and spacings.

In particular, when designing coplanar circuits to operate at 200 GHz on a 75-μm thick InP subtrate with backside groundplane, it is very important to control parallel-plate mode and higher order co-planar mode propagation and generation at circuit discontinuities. In the present work, multi-mode s-parameter matrices for transmission lines and discontinuities, derived using the HP-HFSS simulator, were used to determine the frequencies and line dimensions at which the COPLAN element models were valid. They were also used to estimate under what conditions the effects of higher order modes were expected to be significant. In order to minimize higher order mode coupling at the coplanar tee-junction, airbridge cross-overs or ground plane under-passes were used to equalize the ground potentials at the

Manuscript received August 8, 2000; revised November 29, 2000.

J. W. Archer is with CSIRO Telecommunications and Industrial Physics, Epping NSW 1710, Australia (e-mail: john-archer@tip.csiro.au).

R. Lai, R. Grundbacher, M. Barsky, R. Tsai, and P. Reid are with TRW Telecommunication Programs Division, Redondo Beach, CA 90278 USA.

Publisher Item Identifier S 1531-1309(01)01960-2.

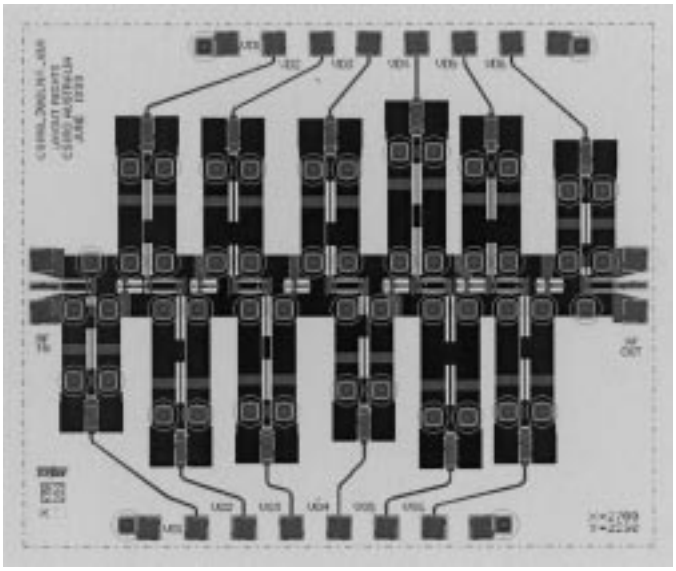

Fig. 1. Circuit layout for 180–205 GHz, six-stage InP HEMT MMIC amplifier (chip size 2.7×2.25 mm)

input line interfaces. The propagation of higher-order coplanar modes was suppressed by limiting the widths of the ground conductors to 100 μm. Through-substrate vias, which connected the coplanar ground strips to the back-side ground plane, were used to suppress the unwanted, parasitic parallel-plate mode as well as helping control higher order coplanar modes. The work reported in this paper represents the first independent application and verification of the accuracy of the COPLAN software at 200 GHz and on InP, since the models had only been previously verified by IMST up to 70 GHz on GaAs substrates.

The InP HEMT devices had a gate length of 0.1 μm and a two-finger, interdigitated geometry with a total width of 20 μm. The small signal HEMT models were developed by CSIRO, using on-wafer s-parameter data from carefully designed on-wafer calibration and device embedding circuits provided by TRW. The models were checked by comparison with appropriately scaled versions of TRW-developed models for devices with a four-finger geometry with a total width of 40 μm. These TRW standard models have been previously verified, to frequencies above 120 GHz, through design and evaluation of a range of amplifier circuits [7]–[8]. The impedance matching and interstage coupling circuits used sections of coplanar waveguide with a 60-μm ground-to-ground spacing and center strip widths ranging from 10 μm to 50 μm. Four-finger interdigitated capacitors with a finger length of 60 μm and spacing of 5 μm were used for interstage decoupling. DC bias was connected to each HEMT gate and drain terminal via low-pass filters constructed from high and low impedance sections of coplanar line. Varying the length of the first, high-impedance line section of the filters as part of the matching networks helped achieve the desired amplifier response. In these filters, the ground-to-ground spacing was 45 μm and the line widths ranged from 5 μm to 35 μm. Each gate and drain low-pass filter is connected to the probe pad via a 66 Ω series resistor and a 1.6 pF thin-film capacitor to ground, in order to improve amplifier stability at frequencies below the operating range.

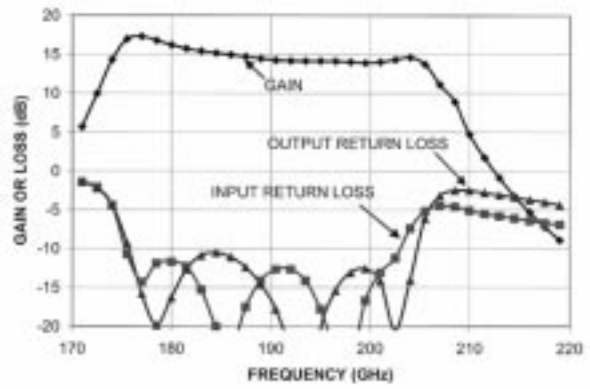

Fig. 2. Predicted performance of the 180–205 GHz, MMIC amplifier.

The predicted performance of the amplifier is shown in Fig. 2. The amplifier was designed to have a gain of 15 dB and input and output return losses were expected to be better than 10 dB over the 175–205 GHz range. The circuit was expected to be unconditionally stable over the entire 1 GHz–250 GHz spectrum. For this first-pass design, excellent agreement has been achieved between the predicted characteristics and measured results. The measurements were made on-wafer for each of the four production wafers delivered to CSIRO. Each wafer contains 11 180–205 GHz amplifier chips of this design. All of the circuits on the wafers have so far been characterized using the wafer prober. Scattering parameter measurements were made using an in-house designed and constructed 180–220 GHz transmission/reflection (T/R) test system which works with an HP8510C network analyzer system and 140–220 GHz coaxial on-wafer probes manufactured by GGB Industries. The T/R test system incorporates a frequency multiplier source, waveguide isolators, and directional couplers and harmonic mixers to provide down-conversion to an IF of 20 MHz for the HP8510C. The network analyzer system provides the local oscillator signals for the system. On-wafer measurements of return and transmission loss with a 25 dB dynamic range are possible with this system. Typical measured performance of one of the amplifiers is shown in Fig. 3, with each stage of the amplifier biased at 1.0 V drain supply voltage and with drain current in the range 1–3 mA, optimized to give the best frequency response.

The agreement between the predicted response and the measurements, verifies that the COPLAN passive element models can be used to accurately design amplifiers in the 200 GHz range provided their range of validity is carefully assessed using e-m simulation studies. For this amplifier, the measured -3 dB bandwidth is from below 180 GHz to 205 GHz (the limited frequency coverage of the test system prevents measurement of the response below 180 GHz). The gain is 14.0 dB $\pm$ 1.5 dB over the 180–200 GHz range. The input return loss is better than 10 dB over the same range and is close to 15 dB between 185 and 200 GHz. The output return loss is between 8 and 10 dB between 180 and 200 GHz.

The noise figure of this amplifier, operating at room-temperature, was estimated using a Y-factor approach. These measurements were made directly at the wafer level by varying the CW input signal by a known amount. The input power

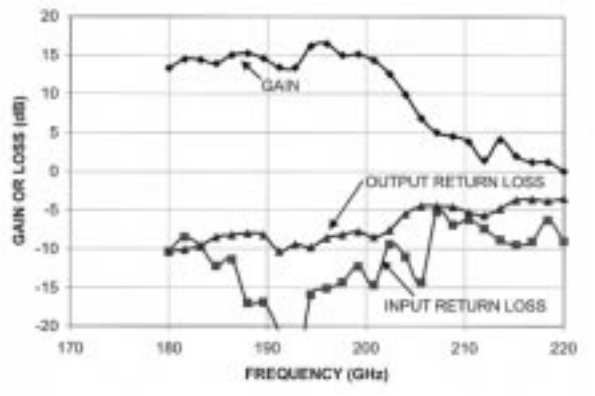

Fig. 3. On-wafer measured performance of a typical 180–205 GHz, MMIC amplifier.

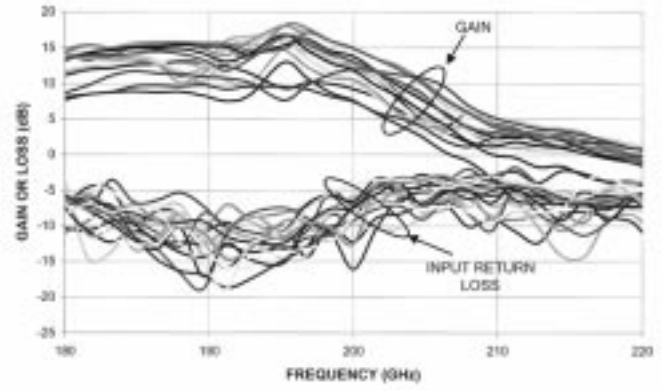

Fig. 4. Measured gain of the nineteen working amplifiers from the best two of the four InP wafers. Also shown is the input return loss of these amplifiers.

TABLE I
ESTIMATED NOISE FIGURE OF THE AMPLIFIER MEASURED ON-WAFER

FREQUENCY (GHz)	ESTIMATED NOISE FIGURE (dB)
185	12.0 ± 4
190	11.5 ± 4
195	12.5 ± 4

level was determined using a calorimeter power meter and the output noise and signal power from the amplifier were measured using a power meter after downconversion and amplification at 20 MHz. The system was calibrated to account for losses in the probes and waveguide assemblies. Waveguide full-band isolators were used between the on-wafer probes and the measurement system to minimize errors due to reflections. The estimated noise figure of the test amplifier (measured S-parameters given in Fig. 3) at three different frequencies in the operating band is given in Table I, under the same bias conditions as before. It is estimated that the measured noise figure is accurate to within ± 4 dB.

Fig. 4 illustrates the measured gain and input return loss of the 19 working amplifiers, from a total of 22, on the best two wafers. This data was taken for all amplifier stages biased at 1.0 V drain supply voltage and 1–3 mA drain current, similar conditions to those used for the measurements shown in Fig. 3. The overall yield of working devices for all four wafers was 33 out of 44 or 75%. The data provides a measure of the uniformity of the amplifier characteristics across a wafer that can currently be achieved at in the 200 GHz band with TRW's 0.1 μm InP HEMT MMIC process. It can be seen that there is a moderate spread in device performance. Although the frequency response of each amplifier covers a similar range, there is a significant variation in average gain. Simulations show that this is most likely due to variations in gate length—a 10% increase in gate length would result in a 5 dB drop in overall amplifier gain.

IV. SUMMARY

This paper has described the design, fabrication and test of a very high performance, InP-based HEMT MMIC amplifier for the 180–205 GHz band. For the first time, it has been demonstrated that commercially-available design tools, if intelligently applied, can be used to achieve first-pass design success for amplifiers at 200 GHz, fabricated using a standard 0.1–μm InP HEMT foundry process. The combination of wide bandwidth, high gain, good gain flatness, and excellent input and output match mean that this MMIC out-performs the only other design that has been reported in the literature in this frequency range [4].

ACKNOWLEDGMENT

J. Archer would like to thank S. Mahon for help with the circuit layout. The authors would like to thank the TRW InP pilot line engineers and laboratory, D. Streit, T. Block, and the MBE area, Po-Hsin and the EBL area, R. Elmajarian, R. Rodriguez, and the InP backside area, and others from Semiconductor Products Center that contributed to this work.

REFERENCES

[1] P. D. Chow *et al.*, "W-band and D-band low noise amplifiers using pseudomorphic InAlAs/InGaAs/InP HEMTs," in *Proc. IEEE Int. Micr. Symp.*, Albuquerque, NM, June 1992, p. 807.
[2] M. Wojtowicz *et al.*, "305 GHz f_t using 0.1 μm g01ate-length graded channel pseudomorphic InAlGaAs/InAlAs HEMTs," *IEEE Electron Device Lett.*, vol. 16, p. 477, Nov. 1994.
[3] Y. L. Kok *et al.*, "160–190 GHz monolithic low-noise amplifiers," *IEEE Microwave Guided Wave Lett.*, vol. 9, no. 8, pp. 311–314, Aug. 1999.
[4] S. Weinreb *et al.*, "High-gain 150–215 GHz MMIC Amplifier with integral waveguide transitions," *IEEE Microwave Guided Wave Lett.*, vol. 9, no. 7, pp. 282–284, July 1999.
[5] R. Lai *et al.*, "0.1 μm InGaAs/InAlAs/InP HEMT production process for high performance and high volume mm-wave applications," in *Proc. GaAs Mantech*, Vancouver, Canada, 1999.
[6] R. Lai *et al.*, "0.15 μm InGaAs/AlGaAs/GaAs HEMT production process for high performance V-band power MMICs," in *GaAs IC Symp.*, San Diego, CA, Oct. 1995, p. 105.
[7] R. Lai *et al.*, "D-band MMIC LNA's with 12 dB gain at 155 GHz fabricated on a high yield InP HEMT production process," *Microw. J.*, p. 166, Sept. 1997.
[8] H. Wang *et al.*, "A 140 GHz monolithic low noise amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 150–152, May 1995.